TS4855

LOUDSPEAKER & HEADSET DRIVER WITH VOLUME CONTROL

- **OPERATING FROM V_{CC} = 3.0 V to 5.0 V**
- **SPEAKER: Mono, THD+N @ 1 kHz is 1% Max @ 1 W into 8 Ω BTL**
- **HEADSET: Stereo, THD+N @ 1 kHz is 0.5% Max. @ 85 mW into 32 Ω BTL**
- **VOLUME CONTROL: 32-step digital volume control**
- **OUTPUT MODE: Eight different selections**
- **Ultra low pop-and-click**
- **Low Shutdown Current (0.1 µA, typ.)**
- **Thermal Shutdown Protection**
- **FLIP-CHIP Package 18 X 300 µm Bumps**
- **TS4855E IJT Lead-Free option available**

DESCRIPTION

The TS4855 is a complete low power audio amplifier solution targeted at mobile phones. It integrates, into an extremely compact flip-chip package, an audio amplifier, a speaker driver, and a headset driver.

The Audio Power Amplifier can deliver 1.1 W (typ.) of continuous RMS output power into an 8 Ω speaker with a 1% THD+N value. To the headset driver, the amplifier can deliver 85 mW (typ.) per channel of continuous average power into stereo 32 Ω bridged-tied load with 0.5% THD+N @ 5 V.

This device features a 32-step digital volume control and 8 different output selections. The digital volume and output modes are controlled through a three-digit SPI interface bus.

APPLICATIONS

- Mobile Phones

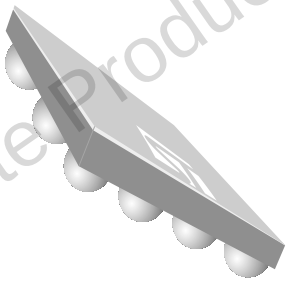
ORDER CODE

Part Number	Temperature Range	Package
		J
TS4855IJT	-40, +85°C	•
TS4855EIJT	-40, +85°C	•

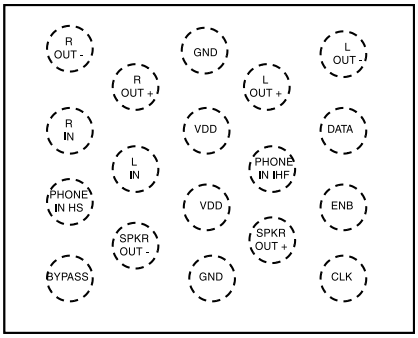
J = Flip Chip Package - only available in Tape & Reel (JT))

PIN CONNECTIONS (top view)

TS4855IJT - Flip Chip

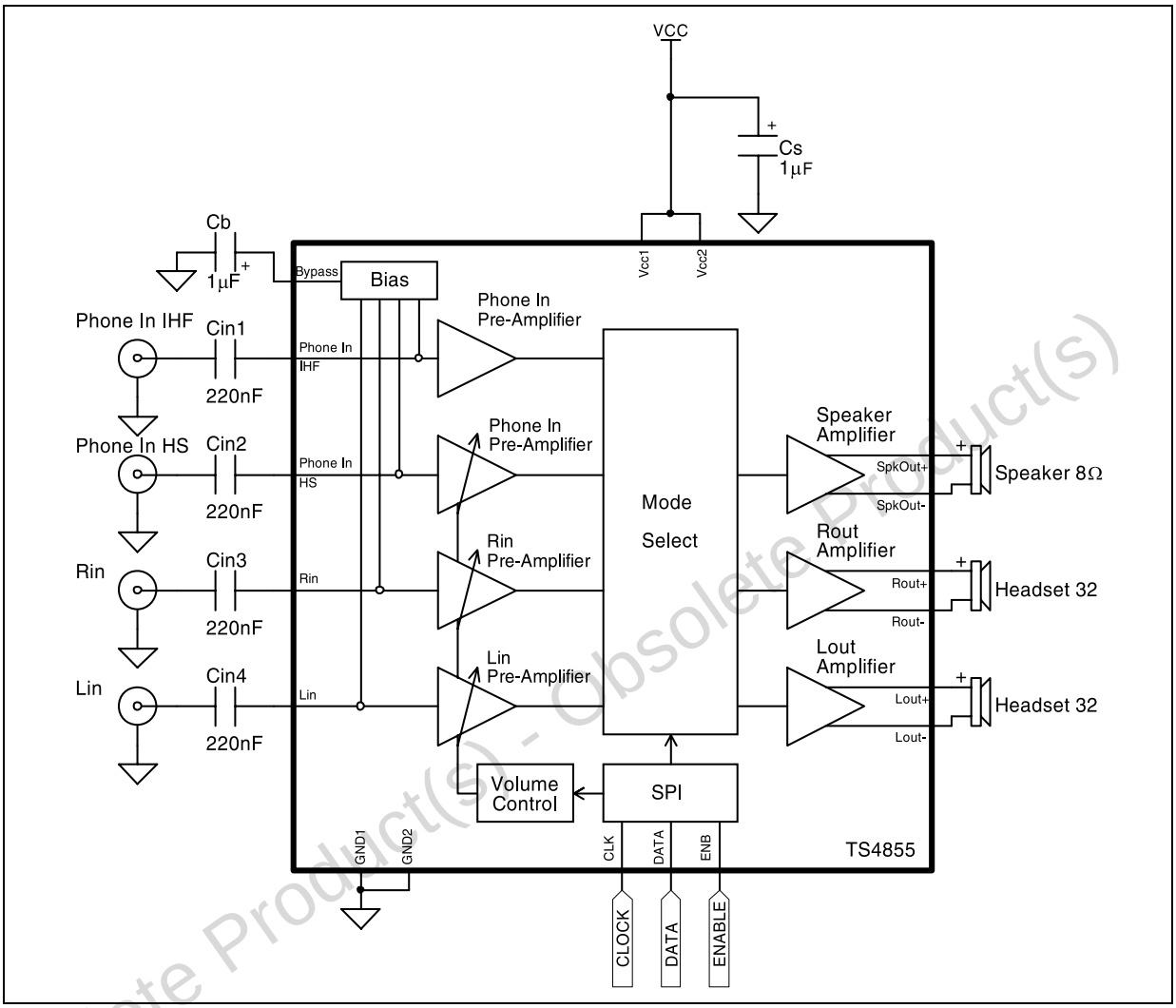


Pin Out (top view)



March 2004

1 APPLICATION INFORMATION FOR A TYPICAL APPLICATION



External component descriptions

Component	Functional Description
C_{in}	This is the input coupling capacitor. It blocks the DC voltage at, and couples the input signal to the amplifier's input terminals. Cin also creates a highpass filter with the internal input impedance Zin at Fc = 1 / (2π x Zin x Cin).
C_S	This is the Supply Bypass capacitor. It provides power supply filtering.
C_B	This is the Bypass pin capacitor. It provides half-supply filtering.

2 SPI BUS INTERFACE

2.1 Pin Descriptions

Pin	Functional Description
DATA	This is the serial data input pin
CLK	This is the clock input pin
ENB	This is the SPI enable pin active at high level

2.2 SPI Operation Description

The serial data bits are organized into a field containing 8 bits of data as shown in *Table 1*. The DATA 0 to DATA 2 bits determine the output mode of the TS4855 as shown in *Table 2*. The DATA 3 to DATA 7 bits determine the gain level setting as illustrated by *Table 3*. For each SPI transfer, the data bits are written to the DATA pin with the least significant bit (LSB) first. All serial data are sampled at the rising edge of the CLK signal. Once all the data bits have been sampled, ENB transitions from logic-high to logic low to complete the SPI sequence. All 8 bits must be received before any data latch can occur. Any excess CLK and DATA transitions will be ignored after the height rising clock edge has occurred. For any data sequence longer than 8 bits, only the first 8 bits will get loaded into the shift register and the rest of the bits will be disregarded.

Table 1: Bit Allocation

	DATA	MODES
LSB	DATA 0	Mode 1
	DATA 1	Mode 2
	DATA 2	Mode 3
	DATA 3	gain 1
	DATA 4	gain 2
	DATA 5	gain 3
	DATA 6	gain 4
MSB	DATA 7	gain 5

Table 2: Output Mode Selection

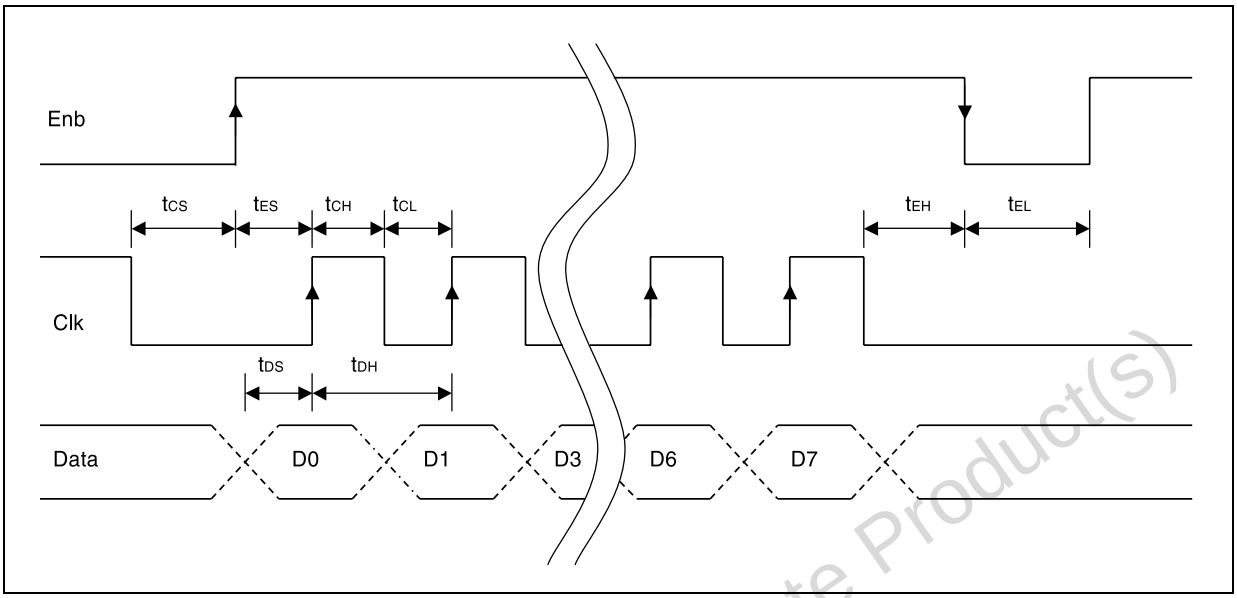
Output Mode #	DATA 2	DATA 1	DATA 0	$SPKR_{out}$	R_{out}	L_{out}
0	0	0	0	SD	SD	SD
1	0	0	1	$+12dBxP_{IHF}$	SD	SD
2	0	1	0	MUTE	$G1xP_{HS}$	$G1xP_{HS}$
3	0	1	1	$+12dBxP_{IHF}$	$G1xP_{HS}$	$G1xP_{HS}$
4	1	0	0	MUTE	$G2xR_{in}$	$G2xL_{in}$
5	1	0	1	$+12dBxP_{IHF}$	$G2xR_{in}$	$G2xL_{in}$
6	1	1	0	MUTE	$G1xP_{HS}+G2xR_{in}$	$G1xP_{HS}+G2xL_{in}$
7	1	1	1	$+12dBxP_{IHF}$	$G1xP_{HS}+G2xR_{in}$	$G1xP_{HS}+G2xL_{in}$

(SD = Shut Down Mode, P_{HS} = Non Filtered Phone In HS, P_{IHF} = External High Pass Filtered Phone In IHF)

Table 3: Gain Control Settings

G2: Gain (dB)	G1: Gain (dB)	DATA 7	DATA 6	DATA 5	DATA 4	DATA 3
-34.5	-40.5	0	0	0	0	0
-33.0	-39.0	0	0	0	0	1
-31.5	-37.5	0	0	0	1	0
-30.0	-36.0	0	0	0	1	1
-28.5	-34.5	0	0	1	0	0
-27.0	-33.0	0	0	1	0	1
-25.5	-31.5	0	0	1	1	0
-24.0	-30.0	0	0	1	1	1
-22.5	-28.5	0	1	0	0	0
-21.0	-27.0	0	1	0	0	1
-19.5	-25.5	0	1	0	1	0
-18.0	-24.0	0	1	0	1	1
-16.5	-22.5	0	1	1	0	0
-15.0	-21.0	0	1	1	0	1
-13.5	-19.5	0	1	1	1	0
-12.0	-18.0	0	1	1	1	1
-10.5	-16.5	1	0	0	0	0
-9.0	-15.0	1	0	0	0	1
-7.5	-13.5	1	0	0	1	0
-6.0	-12.0	1	0	0	1	1
-4.5	-10.5	1	0	1	0	0
-3.0	-9.0	1	0	1	0	1
-1.5	-7.5	1	0	1	1	0
0.0	-6.0	1	0	1	1	1
1.5	-4.5	1	1	0	0	0
3.0	-3.0	1	1	0	0	1
4.5	-1.5	1	1	0	1	0
6.0	0.0	1	1	0	1	1
7.5	1.5	1	1	1	0	0
9.0	3.0	1	1	1	0	1
10.5	4.5	1	1	1	1	0
12.0	6.0	1	1	1	1	1

2.3 SPI Timing Diagram



3 ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage [1]	6	V
T_{oper}	Operating Free Air Temperature Range	-40 to + 85	°C
T_{stg}	Storage Temperature	-65 to +150	°C
T_j	Maximum Junction Temperature	150	°C
R_{thja}	Flip Chip Thermal Resistance Junction to Ambient [2]	166	°C/W
Pd	Power Dissipation	Internally Limited	
ESD	Human Body Model [3]	2	kV
ESD	Machine Model [4]	100	V
	Latch-up Immunity	200	mA
	Lead Temperature (soldering, 10sec)	250	°C

1) All voltage values are measured with respect to the ground pin.

2) Device is protected in case of over temperature by a thermal shutdown active @ 150°C typ.

3) Human body model, 100pF discharged through a 1.5kΩ resistor into pin of device.

4) This is a minimum Value. Machine model ESD, a 200pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5Ω), into pin to pin of device.

5.) All PSRR data limits are guaranteed by evaluation tests.

4 OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	3 to 5	V
V_{phin}	Maximum Phone In Input Voltage	G_{ND} to V_{CC}	V
V_{Rin}/V_{Lin}	Maximum Rin & Lin Input Voltage	G_{ND} to V_{CC}	V
T_{SD}	Thermal Shutdown Temperature	150	°C

5 ELECTRICAL CHARACTERISTICS

Table 4: Electrical characteristics at VCC = +5.0 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current, all gain @ max settings Output Mode 1, Vin = 0 V, no load Output Mode 1, Vin = 0 V, loaded (8Ω) Output Mode 2,3,4,5,6,7 Vin = 0 V, no loads Output mode 2,3,4,5,6,7 Vin = 0 V, loaded (8Ω, 32Ω)		 4.0 5.5 8.0 10	 8 9 11 12	mA
$I_{STANDBY}$	Standby Current Output Mode 0		 0.75	 2	µA
Voo	Output Offset Voltage (differential) Output Mode 1 to 7, Vin = 0 V, no load, Speaker Out Output Mode 2 to 7 Vin = 0 V, no loads, Headset Out		 5 5	 20 40	mV
Vil	“Logic low” input Voltage	0		0.4	V
Vih	“Logic high” input Voltage	1.4		5	V
Po	Output Power $SPKR_{out}$, RL = 8Ω, THD+N = 1%, f = 1 kHz R_{out} & L_{out}, RL = 32Ω, THD+N = 0.5%, f = 1 kHz	 800 70	 1100 100		mW
THD + N	Total Harmonic Distortion + Noise R_{out} & L_{out}, Po = 70 mW, f = 1 kHz, RL = 32Ω $SPKR_{out}$, Po = 800 mW, f = 1 kHz, RL = 8Ω R_{out} & L_{out}, Po = 50 mW, 20 Hz < f < 20 kHz, RL = 32Ω $SPKR_{out}$, Po = 400 mW, 20 Hz < f < 20 kHz, RL = 8Ω		 0.5 0.5 0.5	 1 	%
SNR	Signal To Noise Ratio A-Weighted, f = 1 kHz		80		dB
PSRR[5)]	Power Supply Rejection Ratio $SPKR_{out}$;Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Gain (BTL) = 12 dB, Output mode 1,3,5,7 R_{out}& L_{out};Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output mode 2,3 R_{out}& L_{out};Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output mode 4,5 R_{out}& L_{out};Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output mode 6,7	 58 52 50 46	 62 61 58 53		dB
G2	Digital Gain Range (Rin & Lin) to R_{out}, L_{out}	-34.5		12	dB
G1	Digital Gain Range (Phone In HS) to R_{out}, L_{out}	-40.5		6	dB
	Digital Gain Stepsize		1.5		dB
	Stepsize Error		± 0.6		dB

Table 4: Electrical characteristics at VCC = +5.0 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
	Phone In Volume BTL maximum GAIN from Phone In HS to R_{out}, L_{out} BTL minimum GAIN from Phone In HS to R_{out}, L_{out}	 5.4 -41.1	 6 -40.5	 6.6 -39.9	dB
	Phone In Volume BTL maximum gain from Rin, Lin to R_{out}, L_{out} BTL minimum gain from Rin, Lin to R_{out}, L_{out}	 11.4 -35.1	 12 -34.5	 12.6 -33.9	dB
	Phone In Volume BTL gain from Phone In IHF to $SPKR_{out}$	11.4	12	12.6	dB
Zin	Phone In IHF Input Impedance	16	20	24	kΩ
Zin	Phone In HS, Rin & Lin Input Impedance, All Gain setting	42.5	50	57.5	kΩ
tes	Enable Step up Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

Table 5: Electrical characteristics at VCC = +3.0 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current, all gain @ max settings Output Mode 1, Vin = 0 V, no load Output Mode 1, Vin = 0 V, loaded (8Ω) Output Mode 2,3,4,5,6,7 Vin = 0 V, no loads Output mode 2,3,4,5,6,7 Vin = 0 V, loaded (8Ω, 32Ω)		 3.5 4.5 7.5 9	 7 8 10 11	mA
$I_{STANDBY}$	Standby Current Output Mode 0		 0.6	 2	µA
Voo	Output Offset Voltage (differential) Output Mode 1 to 7, Vin = 0 V, no load, Speaker Out Output Mode 2 to 7 Vin = 0 V, no loads, Headset Out		 5 5	 20 40	mV
Vil	“Logic low” input Voltage	0		0.4	V
Vih	“Logic high” input Voltage	1.4		3	V

Table 5: Electrical characteristics at VCC = +3.0 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
Po	Output Power $SPKR_{out}$, RL = 8Ω, THD = 1%, f = 1 kHz R_{out} & L_{out}, RL = 32Ω, THD = 0.5%, f = 1 kHz	 300 20	 340 25		mW
THD + N	Total Harmonic Distortion + Noise R_{out} & L_{out}, Po = 20 mW, f = 1 kHz, RL = 32Ω $SPKR_{out}$, Po = 300 mW, f = 1 kHz, RL = 8Ω R_{out} & L_{out}, Po = 15 mW, 20 Hz < f < 20 kHz, RL = 32Ω $SPKR_{out}$, Po = 250 mW, 20 Hz < f < 20 kHz, RL = 8Ω		 0.5 0.5	 0.5 1	%
SNR	Signal To Noise Ratio A-Weighted, f = 1 kHz		80		dB
PSRR [5]	Power Supply Rejection Ratio $SPKR_{out}$,Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Gain (BTL) = 12 dB, Output Mode 1,3,5,7 R_{out} & L_{out} Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output Mode 2,3 R_{out} & L_{out} Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output Mode 4,5 R_{out} & L_{out} Vripple = 200 mV Vpp, F = 217 Hz, Input Terminated 50Ω Maximum gain setting, Output Mode 6,7	 58 52 49 45	 62.5 56.5 55 49.5		dB
G2	Digital Gain Range - Rin & Lin to R_{out} ,L_{out}	-34.5		12	dB
G1	Digital Gain Range - Phone In HS to R_{out} ,L_{out}	-40.5		6	dB
	Digital Gain stepsize		1.5		dB
	Stepsize Error		± 0.6		dB
	Phone In Volume BTL maximum GAIN from Phone In HS to R_{out}, L_{out} BTL minimum GAIN from Phone In HS to R_{out}, L_{out}	 5.4 -41.1	 6 -40.5	 6.6 -39.9	dB
	Phone In Volume BTL maximum gain from Rin, Lin to R_{out}, L_{out} BTL minimum gain from Rin, Lin to R_{out}, L_{out}	 11.4 -35.1	 12 -34.5	 12.6 -33.9	dB
	Phone In Volume BTL gain from Phone In IHF to $SPKR_{out}$	 11.4	 12	 12.6	dB
Zin	Phone In IHF Input Impedance, all gains setting	16	20	24	kΩ
Zin	Phone In HS, Rin & Lin Input Impedance, all gains setting	42.5	50	57.5	kΩ
tes	Enable Step up Time - ENB	20			ns
teh	Enable Hold Time - ENB	20			ns
tel	Enable Low Time - ENB	30			ns

Table 5: Electrical characteristics at VCC = +3.0 V, GND = 0 V, Tamb = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
tds	Data Setup Time- DATA	20			ns
tdh	Data Hold Time - DATA	20			ns
tcs	Clock Setup time - CLK	20			ns
tch	Clock Logic High Time - CLK	50			ns
tcl	Clock Logic Low Time - CLK	50			ns
fclk	Clock Frequency - CLK	DC		10	MHz

Index of Graphics

Note: In the graphs that follow, the abbreviations Spkout = Speaker Output, and HDout = Headphone Output are used.

Figure 1: Spkout THD+N vs. output power (Output modes 1, 3, 5, 7)

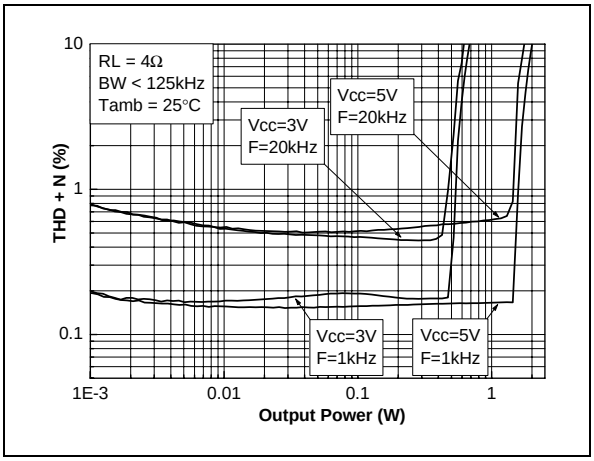


Figure 2: Spkout THD+N vs. output power (Output modes 1, 3, 5, 7)

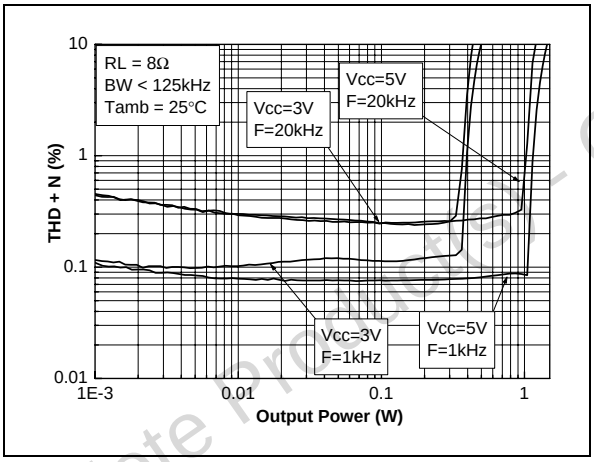


Figure 3: Spkout THD+N vs. output power (Output modes 1, 3, 5, 7)

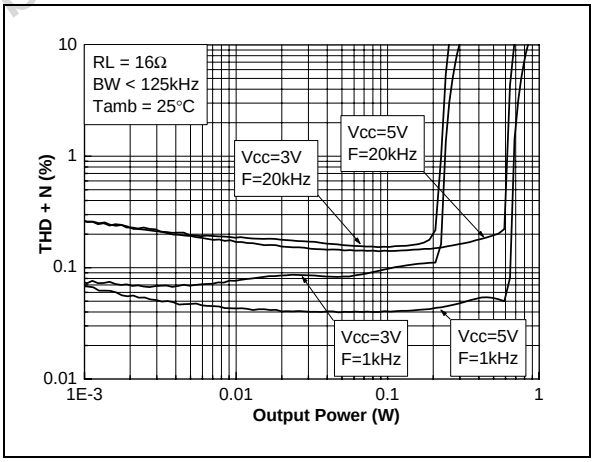


Figure 4: HDout THD+N vs. output power (Output modes 2, 3 G=+6dB)

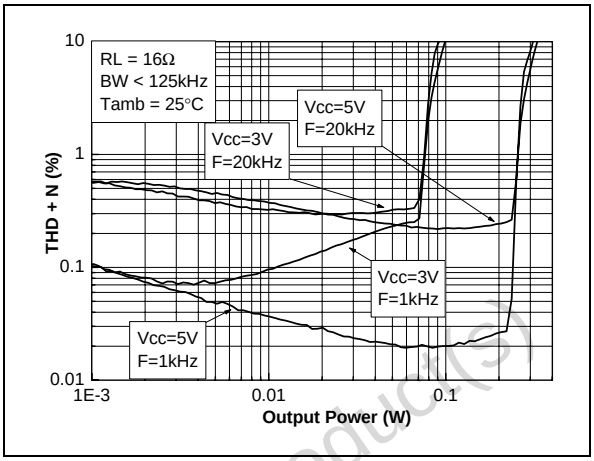


Figure 5: HDout THD+N vs. output power (Output modes 2, 3 G=+3dB)

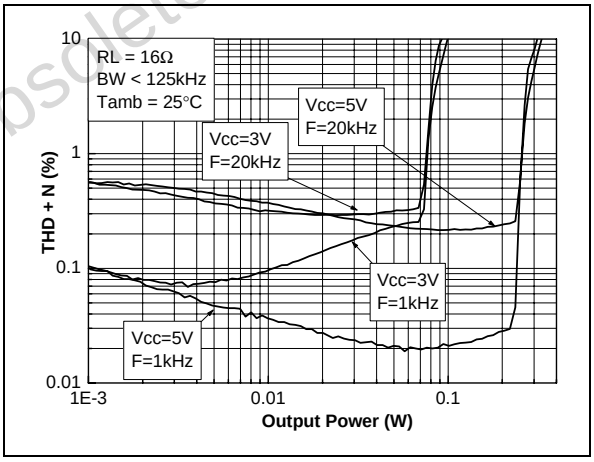


Figure 6: HDout THD+N vs. output power (Output modes 2, 3 G=+6dB)

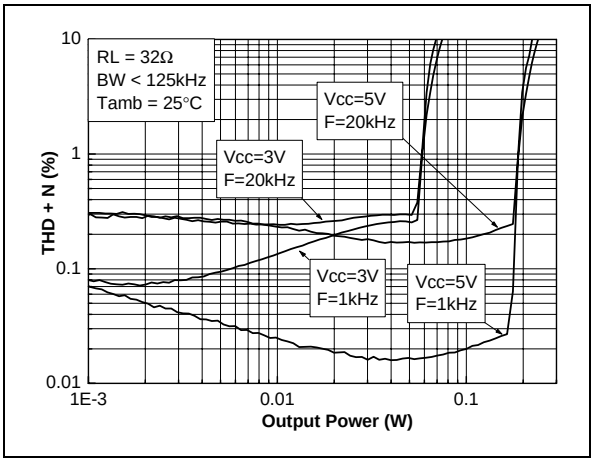


Figure 7: HDout THD+N vs. output power (Output modes 2, 3 G=+3dB)

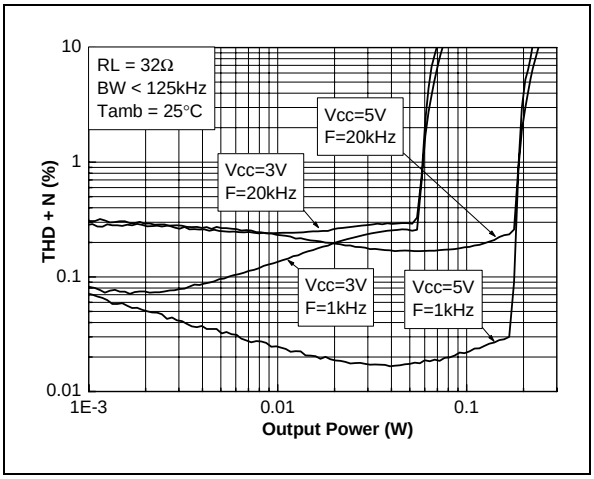


Figure 8: HDout THD+N vs. output power (Output modes 4, 5 G=+12dB)

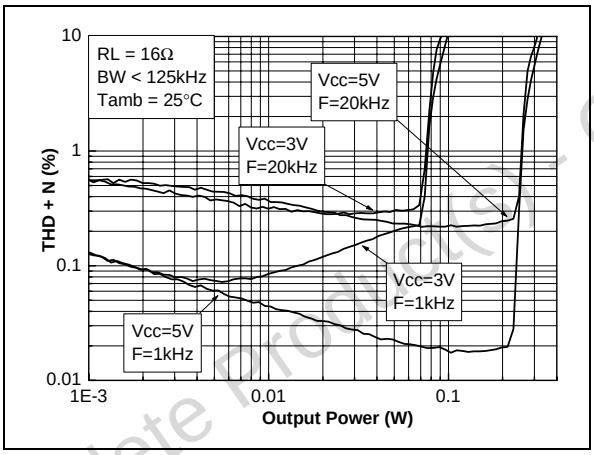


Figure 9: HDout THD+N vs. output power (Output modes 4, 5 G=+6dB)

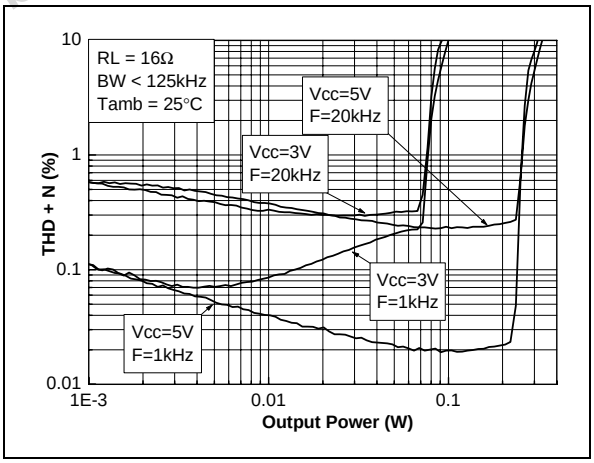


Figure 10: HDout THD+N vs. output power (Output modes 4, 5 G=+12dB)

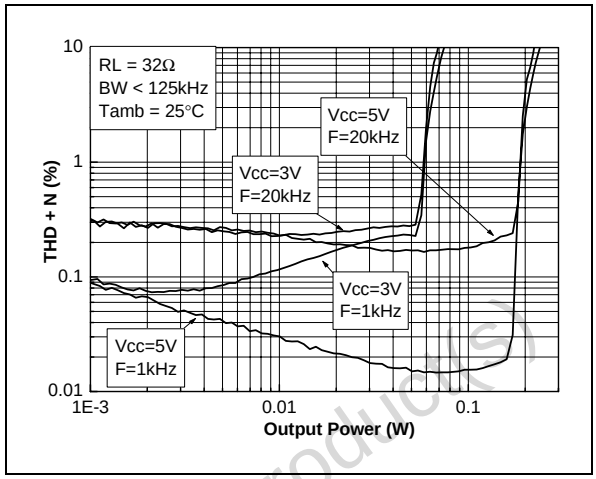


Figure 11: HDout THD+N vs. output power (Output modes 4, 5 G=+6dB)

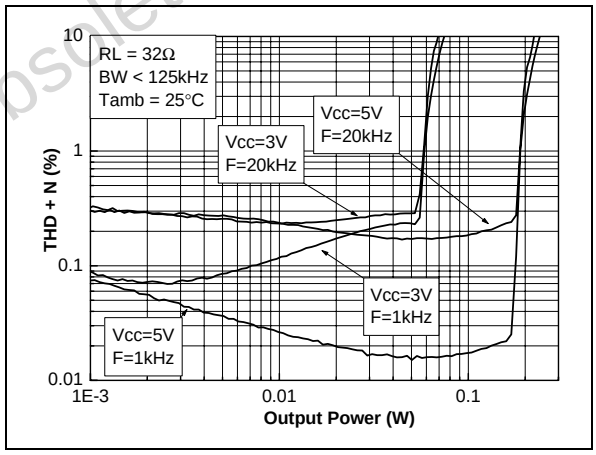


Figure 12: HDout THD+N vs. frequency (Output modes 1, 3, 5, 7)

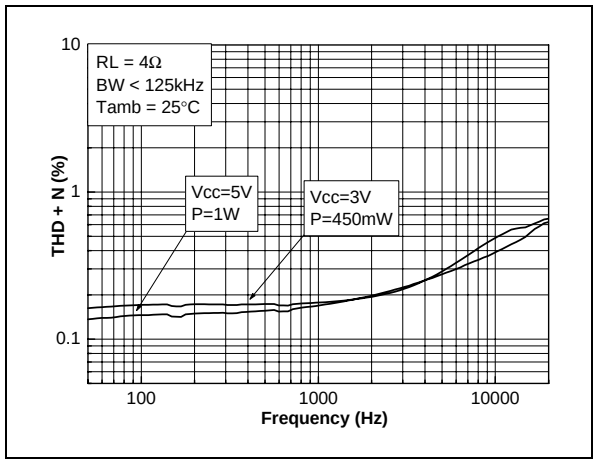


Figure 13: Spkout THD+N vs. frequency (Output modes 1, 3, 5, 7)

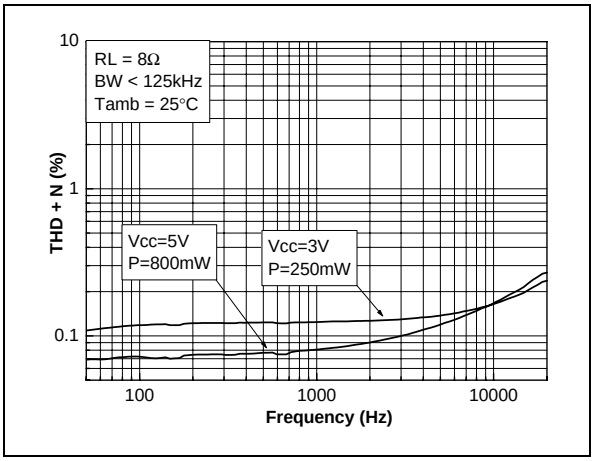


Figure 14: Spout THD+N vs. frequency (Output modes 1, 3, 5, 7)

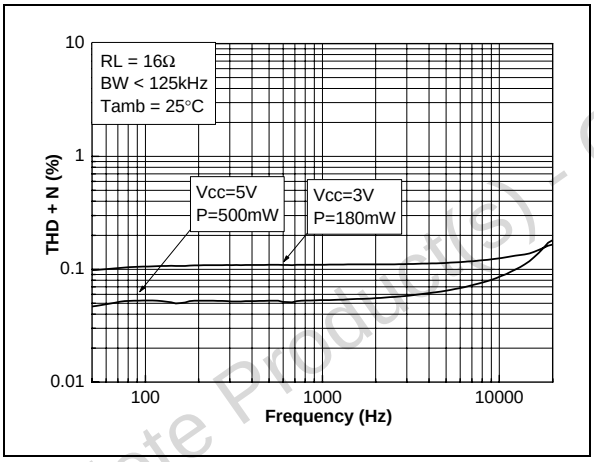


Figure 15: HDout THD+N vs. frequency (Output modes 2, 3 G=+6dB)

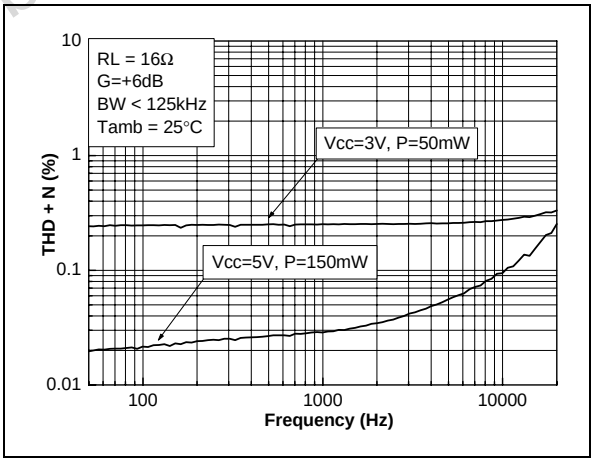


Figure 16: HDout THD+N vs. Frequency (Output modes 2, 3 G=+6dB)

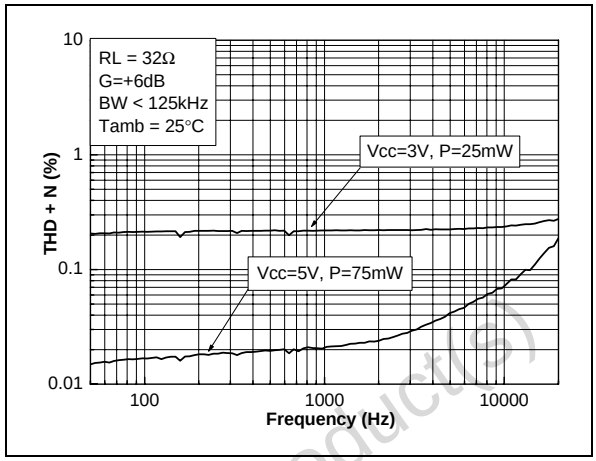


Figure 17: HDout THD+N vs. frequency (Output modes 4, 5 G=+12dB)

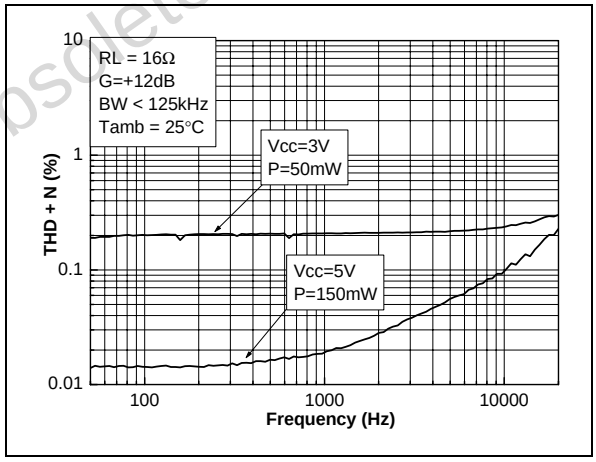


Figure 18: HDout THD+N vs. frequency (Output modes 4, 5 G=+12dB)

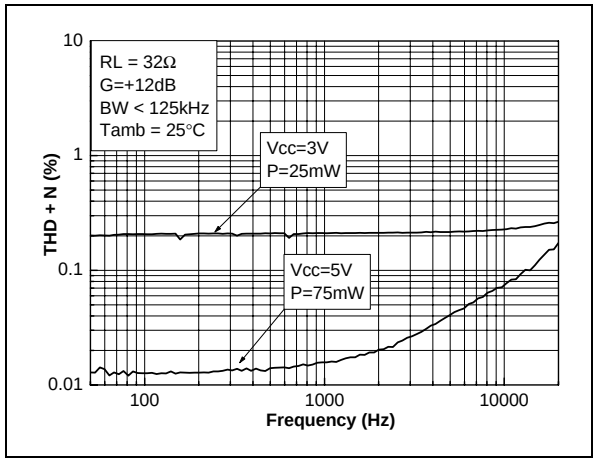


Figure 19: Speaker output power vs. power supply voltage (Output modes 1, 3, 5, 7)

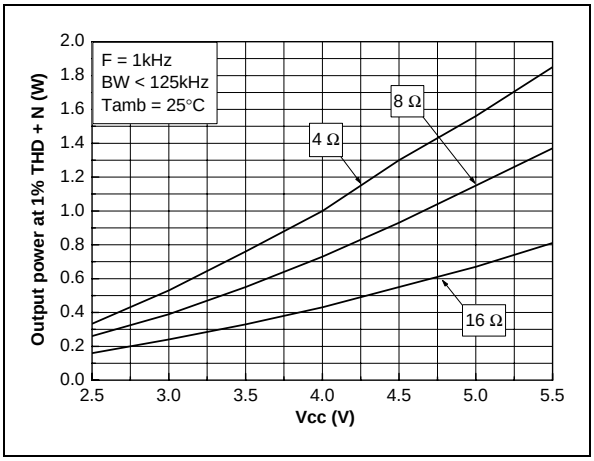


Figure 20: Speaker output power vs. power supply voltage (Output modes 1, 3, 5, 7)

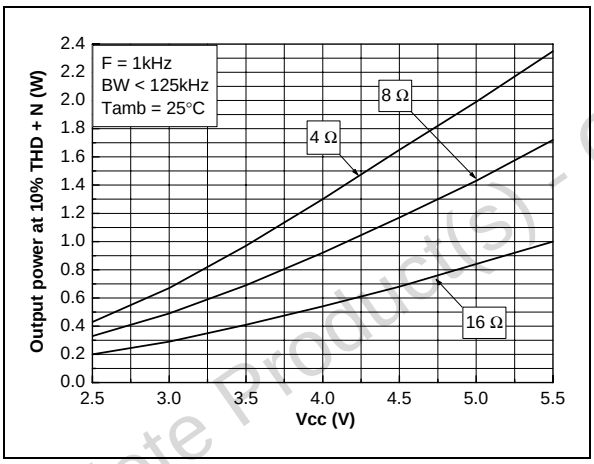


Figure 21: Headphone output power vs. power supply voltage (Output modes 2, 3, 4, 5, 6, 7)

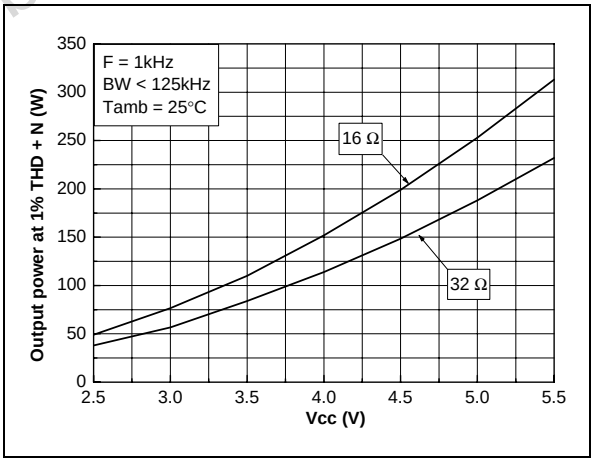


Figure 22: Headphone output power vs. power supply voltage (Output modes 2, 3, 4, 5, 6, 7)

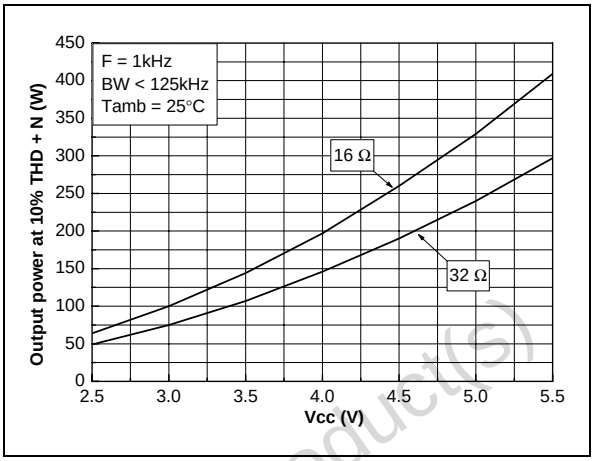


Figure 23: Speaker output power vs. load resistance (Output modes 1, 3, 5, 7)

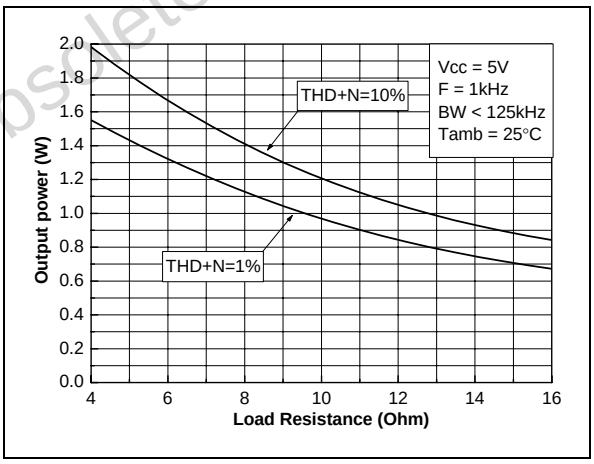


Figure 24: Speaker output power vs. load resistance (Output modes 1, 3, 5, 7)

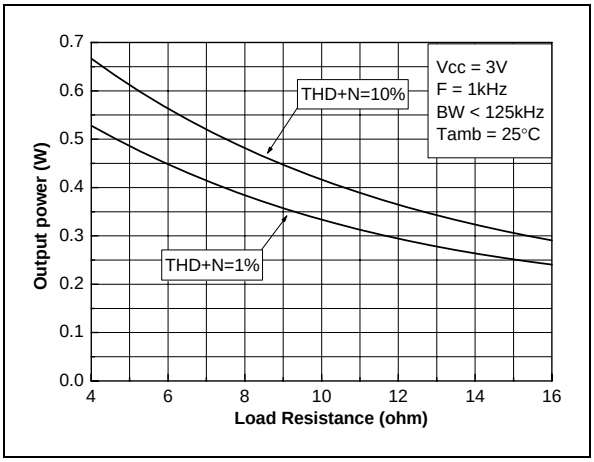


Figure 25: Headphone output power vs. load resistance (Output modes 2, 3, 4, 5, 6, 7)

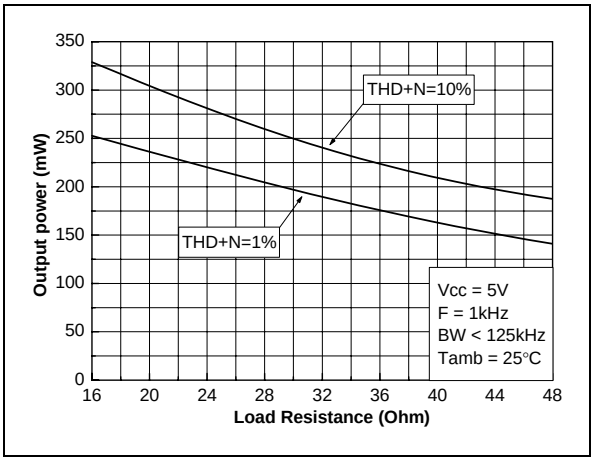


Figure 26: Headphone output power vs. load resistance (Output modes 2, 3, 4, 5, 6, 7)

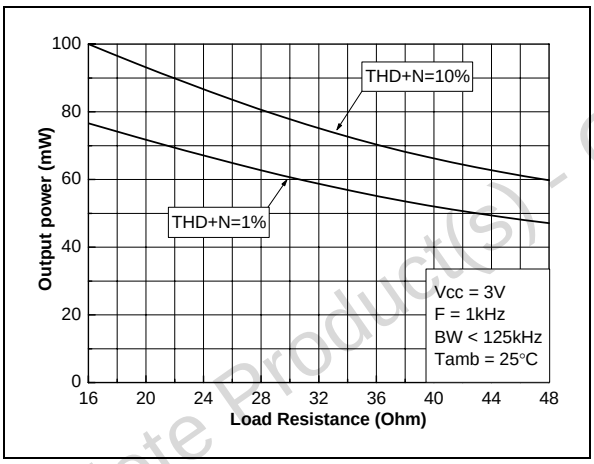


Figure 27: Spkout PSRR vs. frequency (Output modes 1, 3, 5, 7 input grounded)

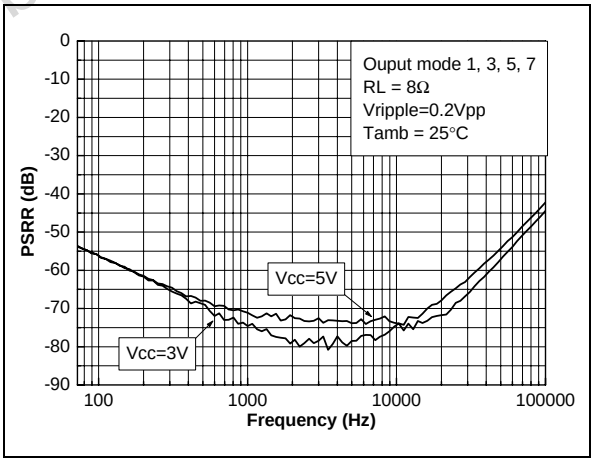


Figure 28: Spkout PSRR vs. frequency (Output modes 2, 4, 6 input grounded)

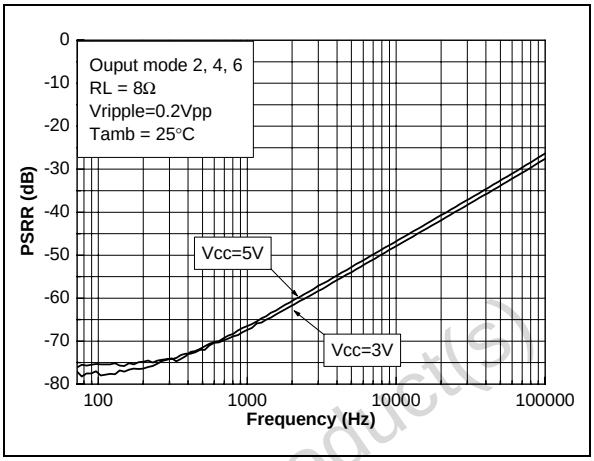


Figure 29: HDout PSRR vs. frequency (Output modes 2, 3 input grounded)

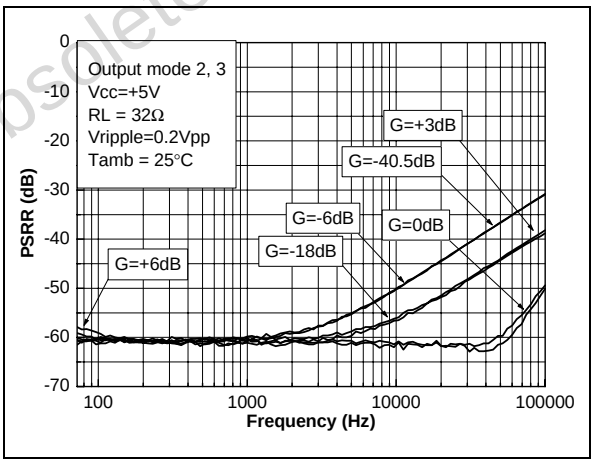


Figure 30: HDout PSRR vs. frequency (Output modes 2, 3 input grounded)

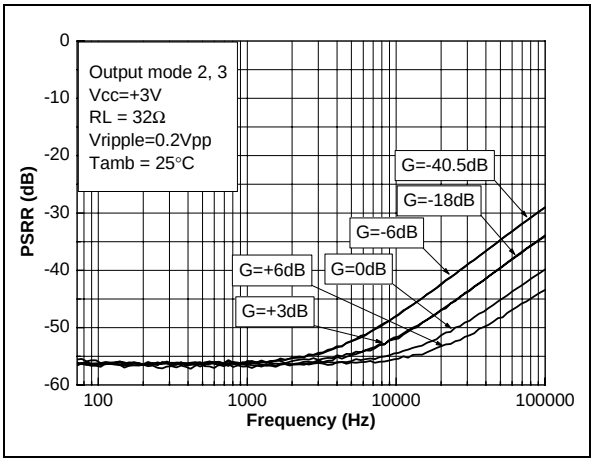


Figure 31: HDout PSRR vs. frequency (Output modes 4, 5 inputs grounded)

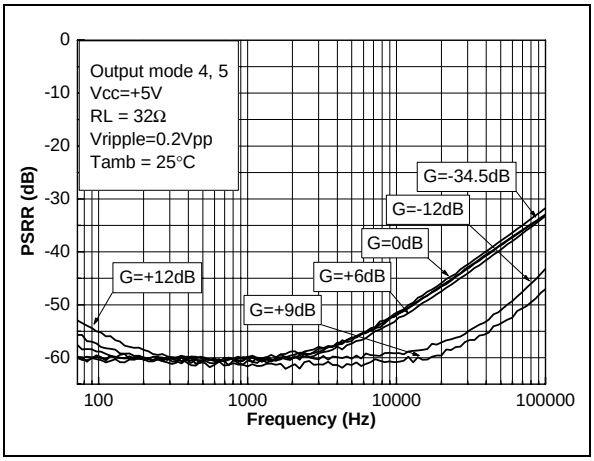


Figure 32: HDout PSRR vs. frequency (Output modes 4, 5 inputs grounded)

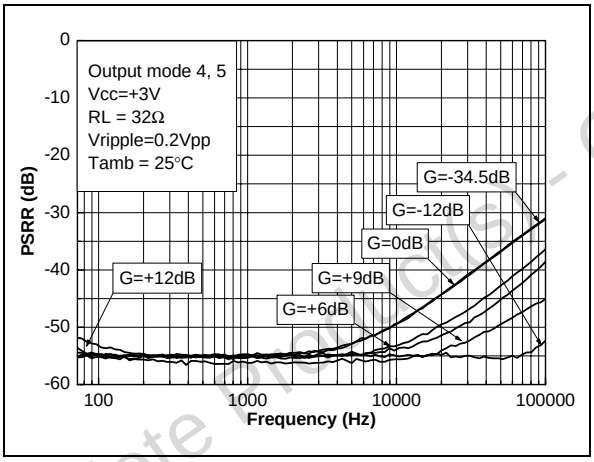


Figure 33: HDout PSRR vs. frequency (Output modes 6, 7 inputs grounded)

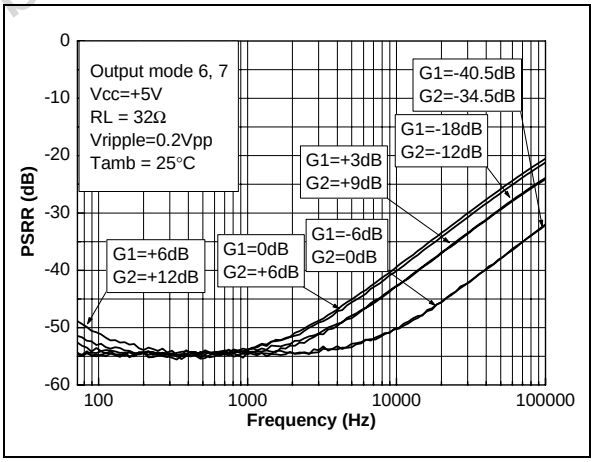


Figure 34: HDout PSRR vs. frequency (Output modes 6, 7 inputs grounded)

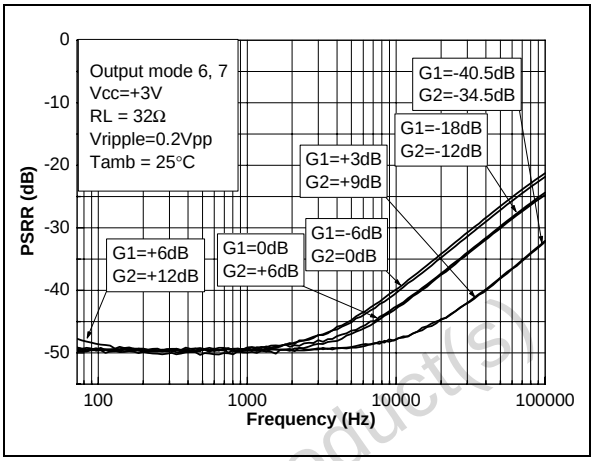


Figure 35: Spkout mute attenuation vs. frequency (Output modes 2, 4, 6)

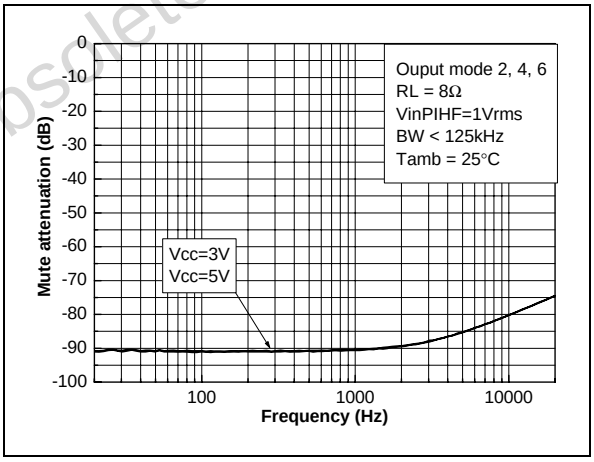


Figure 36: Spkout frequency response (Output modes 1, 3, 5, 7)

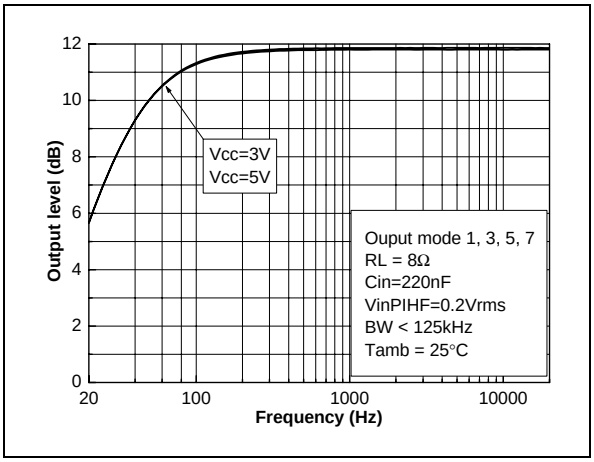


Figure 37: HDout frequency response (Output modes 2, 3 G=+6dB)

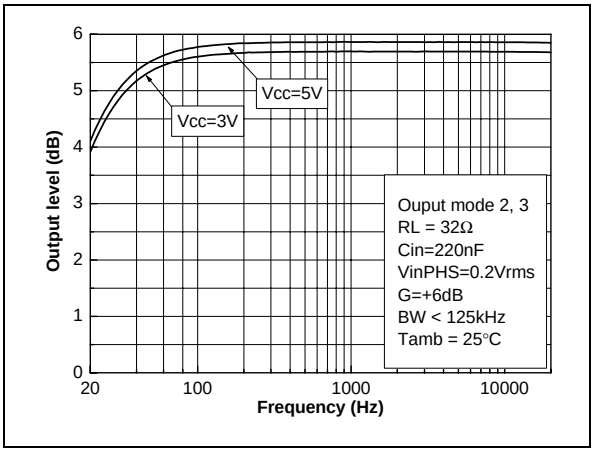


Figure 38: HDout frequency response (Output modes 4, 5 G=+12dB)

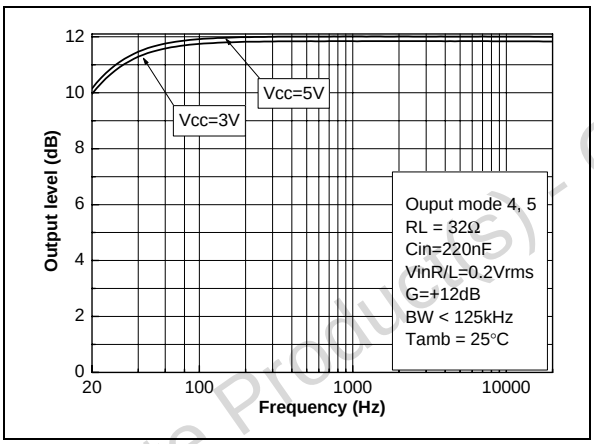


Figure 39: Spkout -3dB lower cut off freq. vs. input capacitor (Output modes 1, 3, 5, 7)

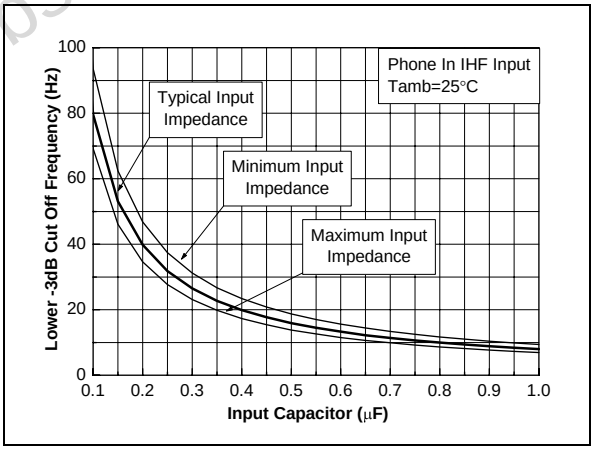


Figure 40: HDout -3dB lower cut-off frequency vs. input capacitor (Output modes 2, 3, 4, 5, 6, 7)

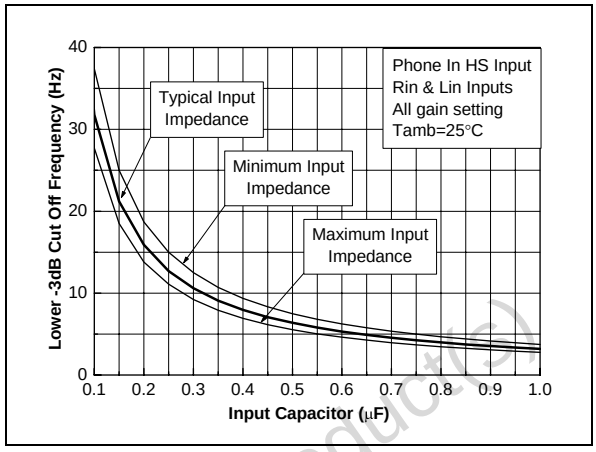


Figure 41: HDout -3dB lower cut-off freq. vs. gain setting (Output modes 2, 3, 4, 5, 6, 7)

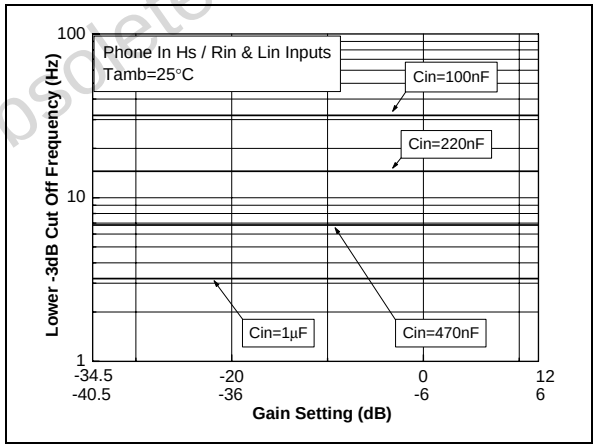


Figure 42: Power derating curves

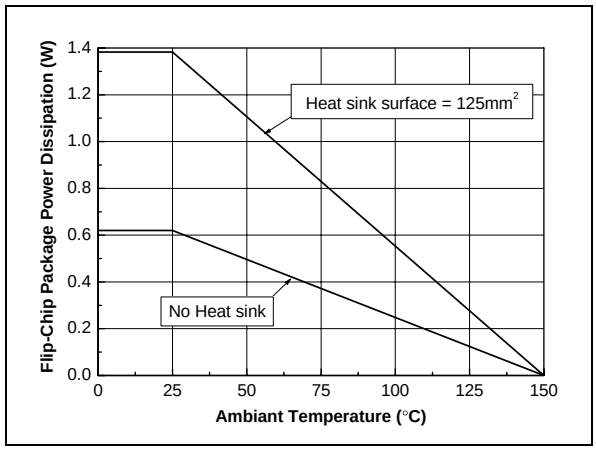


Figure 43: Spkout SNR vs. power supply voltage, unweighted filter, BW = 20 Hz to 20 kHz

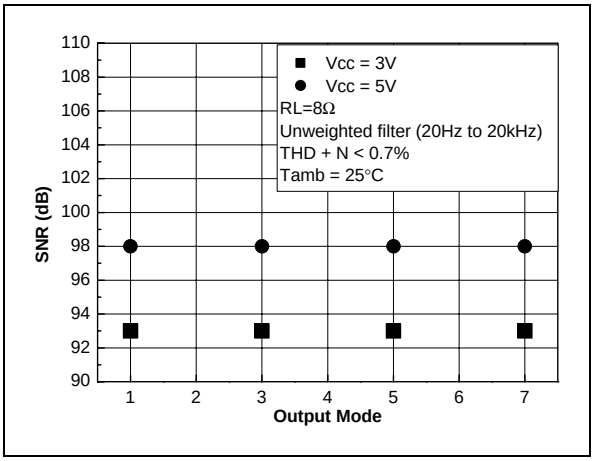


Figure 44: Spkout SNR vs. power supply voltage, weighted filter A, BW = 20 Hz to 20 kHz

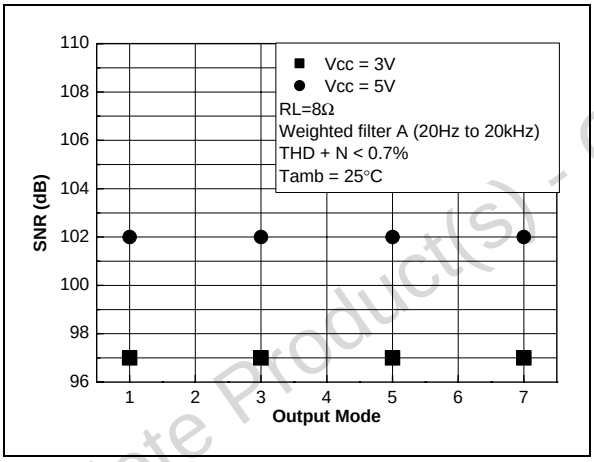


Figure 45: HDout SNR vs. power supply voltage, unweighted filter, BW= 20 Hz to 20 kHz

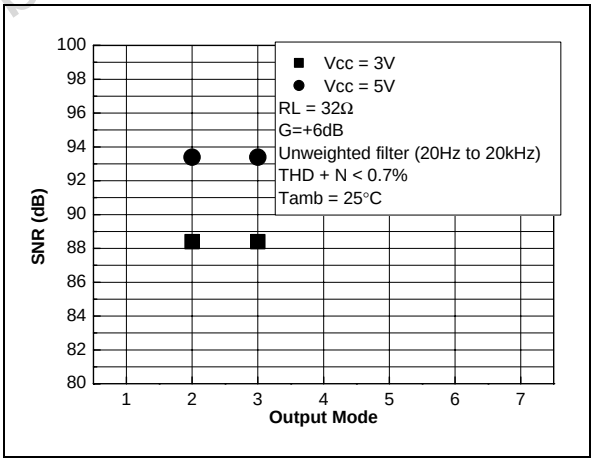


Figure 46: HDout SNR vs. power supply voltage, weighted filter A, BW=20Hz to 20kHz

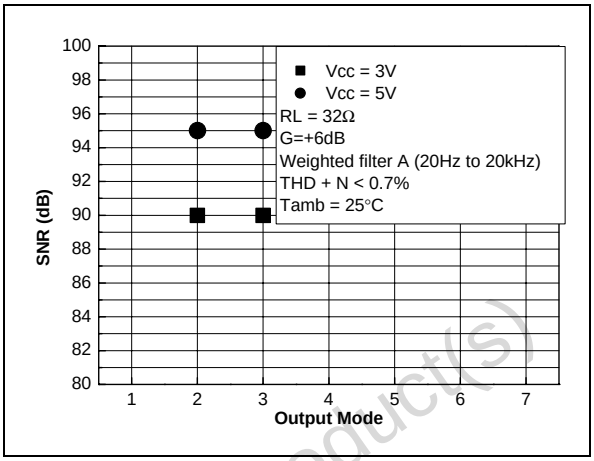


Figure 47: HDout SNR vs. Power supply voltage, unweighted filter, BW=20Hz to 20kHz

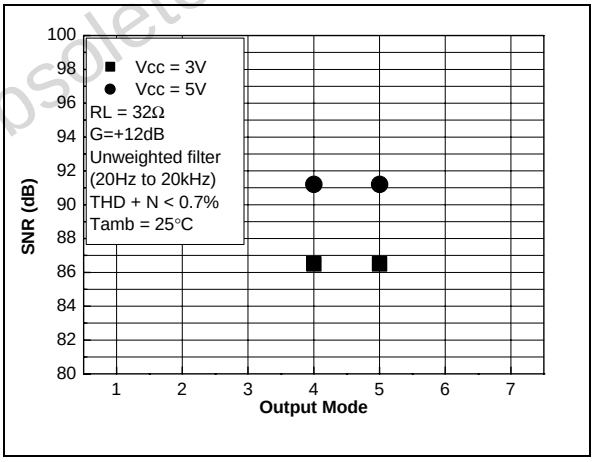


Figure 48: HDout SNR vs. power supply voltage, weighted filter A, BW = 20 Hz to 20 kHz

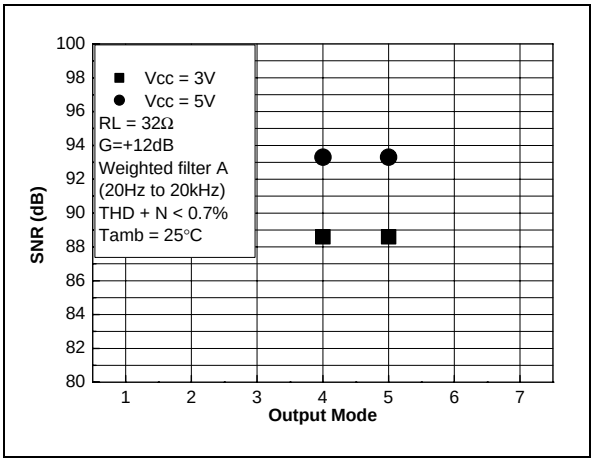


Figure 49: HDout SNR vs. power supply voltage, unweighted filter, BW = 20 Hz to 20 kHz)

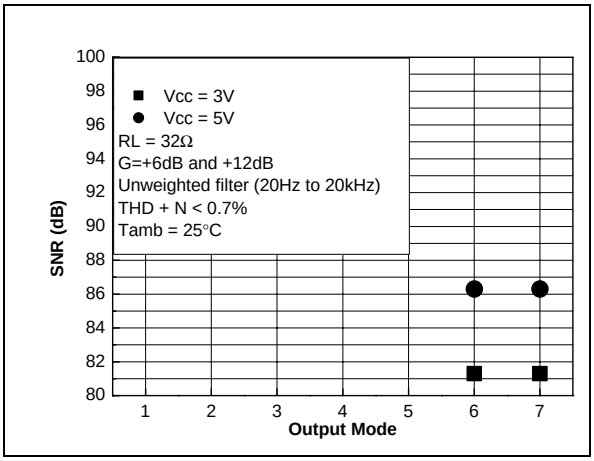


Figure 50: HDout SNR vs. power supply voltage, weighted filter A, BW = 20 Hz to 20 kHz)

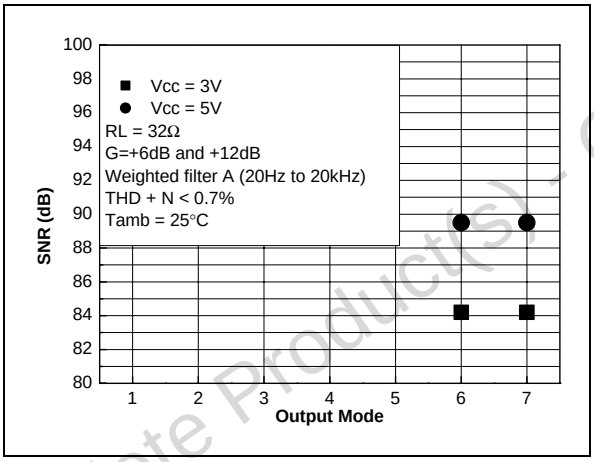


Figure 51: Current consumption vs. power supply voltage

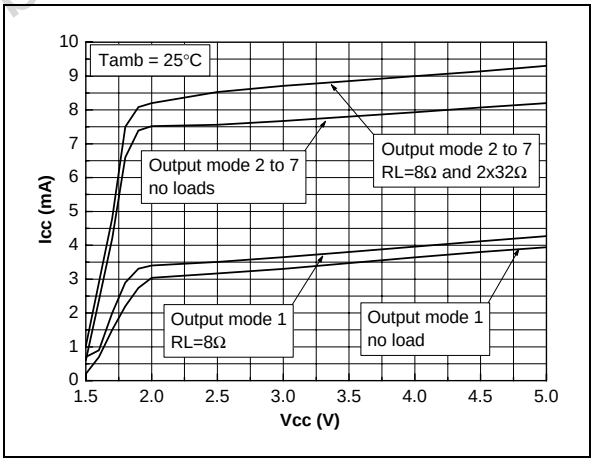


Figure 52: Power dissipation vs. output power: speaker output

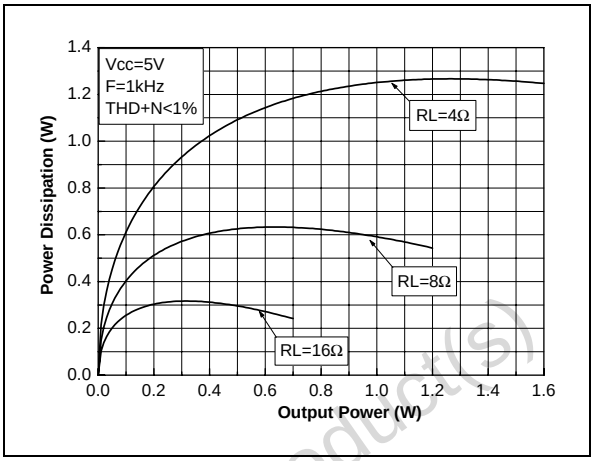


Figure 53: Power dissipation vs. output power: speaker output

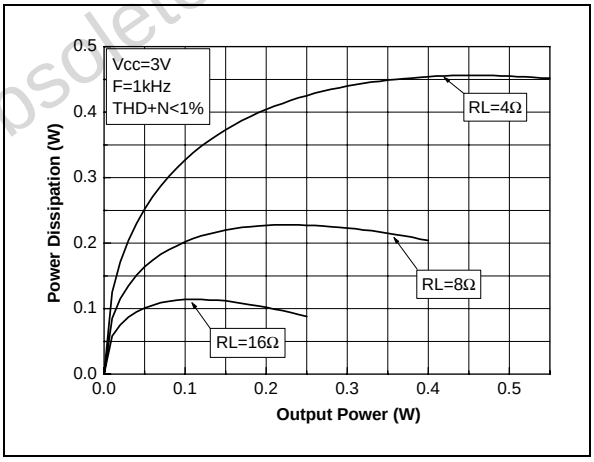


Figure 54: Power dissipation vs. output power. headphone output one channel

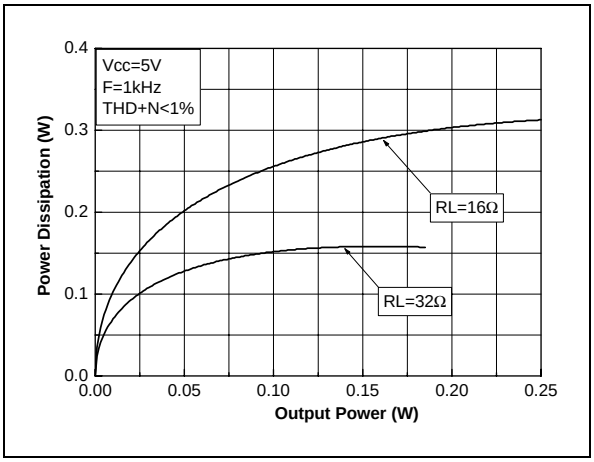
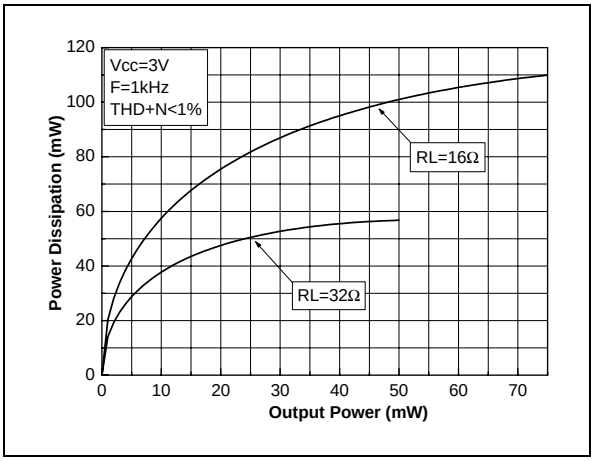


Figure 55: Power dissipation vs. output power. headphone output one channel



6 APPLICATION INFORMATION

6.1 BTL Configuration Principle

The TS4855 integrates 3 monolithic power amplifiers having BTL output. BTL (Bridge Tied Load) means that each end of the load is connected to two single-ended output amplifiers. Thus, we have:

Single ended output 1 = Vout1 = Vout (V)

Single ended output 2 = Vout2 = -Vout (V)

and

Vout1 - Vout2 = 2Vout (V)

The output power is:

$$Pout = \frac{(2\,Vout_{RMS})^2}{R_L} (W)$$

For the same power supply voltage, the output power in BTL configuration is 4 times higher than the output power in single-ended configuration.

6.2 Power dissipation and efficiency

Hypotheses:

- Voltage and current in the load are sinusoidal (Vout and Iout).
- Supply voltage is a pure DC source (Vcc).

Regarding the load we have:

$$V_{OUT} = V_{PEAK} \sin\omega t \ (V)$$

and

$$I_{OUT} = \frac{V_{OUT}}{R_L} (A)$$

and

$$P_{OUT} = \frac{V_{PEAK}^2}{2R_L} (W)$$

Therefore, the average current delivered by the supply voltage is:

$$I_{CC\ AVG} = 2\frac{V_{PEAK}}{\pi R_L} (A)$$

The power delivered by the supply voltage is:

$$Psupply = Vcc\ Icc_{AVG} (W)$$

Then, the **power dissipated by each amplifier** is Pdiss = Psupply - Pout (W)

$$P_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi\sqrt{R_L}}\sqrt{P_{OUT}} - P_{OUT} \quad (W)$$

and the maximum value is obtained when:

$$\frac{\partial Pdiss}{\partial P_{OUT}} = 0$$

and its value is:

$$Pdiss\,max = \frac{2Vcc^2}{\pi^2 R_L} (W)$$

Note: This maximum value is only depending on power supply voltage and load values.

The **efficiency** is the ratio between the output power and the power supply

$$\eta = \frac{P_{OUT}}{Psupply} = \frac{\pi V_{PEAK}}{4V_{CC}}$$

The maximum theoretical value is reached when Vpeak = Vcc, so

$$\frac{\pi}{4} = 78.5\%$$

The TS4855 has 3 independent power amplifiers and each amplifier produces heat due to its power dissipation. Therefore, the maximum die temperature is the sum of the each amplifier's maximum power dissipation. It is calculated as follows:

$P_{diss\ speaker}$ = Power dissipation due to the speaker power amplifier.

$P_{diss\ head}$ = Power dissipation due to each headphone's power amplifier.

$Total\ P_{diss} = P_{diss\ speaker} + P_{diss\ head1} + P_{diss\ head2}$ (W)

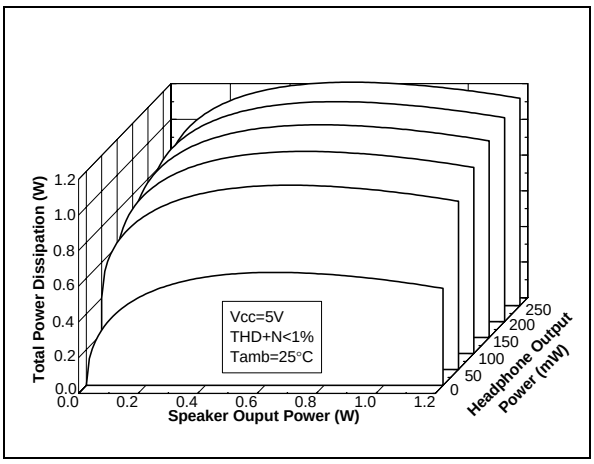
In most cases, $P_{diss\ head1} = P_{diss\ head\ 2}$, giving:

$$Total\ P_{diss} = P_{diss\ speaker} + 2P_{diss\ head} (W)$$

$$TotalP_{diss} = \frac{2\sqrt{2}\,V_{CC}}{\pi}\left[\sqrt{\frac{P_{OUT\ SPEAKER}}{R_{L\ SPEAKER}}} + 2\sqrt{\frac{P_{OUT\ HEAD}}{R_{L\ HEAD}}}\right] - \left[P_{OUT\ SPEAKER} + 2P_{OUT\ HEAD}\right] \quad (W)$$

The following graph shows an example of the previous formula, with Vcc set to +5 V, $R_{load\ speaker}$ set to 8 Ω, and $R_{load\ headphone}$ se to 16 Ω.

Figure 56: Example of total power dissipation vs. speaker and headphone output power



6.3 Low frequency response

In low frequency region, the effect of Cin starts. Cin with Zin forms a high pass filter with a -3 dB cut off frequency.

$$F_{CL} = \frac{1}{2\ \pi\ Zin\ Cin}(Hz)$$

Zin is the input impedance of the corresponding input:

- 20 kΩ for Phone In IHF input
- 50 kΩ for the 3 other inputs

Note: For all inputs, the impedance value remains constant for all gain settings. This means that the lower cut-off frequency doesn't change with gain setting. Note also that 20 kΩ and 50 kΩ are typical values and there are tolerances around these values (see Electrical Characteristics on page 6).

In *Figures 39* to *41*, you could easily establish the Cin value for a -3 dB cut-off frequency required.

6.4 Decoupling of the circuit

Two capacitors are needed to bypass properly the TS4855, a power supply bypass capacitor Cs and a bias voltage bypass capacitor Cb.

Cs has especially an influence on the THD+N in high frequency (above 7 kHz) and indirectly on the power supply disturbances.

With 1 µF, you could expect similar THD+N performances like shown in the datasheet.

If Cs is lower than 1 µF, THD+N increases in high frequency and disturbances on the power supply rail are less filtered.

To the contrary, if Cs is higher than 1 µF, those disturbances on the power supply rail are more filtered.

Cb has an influence on THD+N in lower frequency, but its value is critical on the final result of PSRR with input grounded in lower frequency:

- If Cb is lower than 1 µF, THD+N increases at lower frequencies and the PSRR worsens upwards.
- If Cb is higher than 1 µF, the benefit on THD+N and PSRR in the lower frequency range is small.

6.5 Startup time

When the TS4855 is controlled to switch from the full standby mode (output mode 0) to another output mode, a delay is necessary to stabilize the DC bias. This delay depends on the Cb value and can be calculated by the following formulas.

Typical startup time = 0.0175 x Cb (s)

Max. startup time = 0.025 x Cb (s)
(Cb is in µF in these formulas)

These formulas assume that the Cb voltage is equal to 0 V. If the Cb voltage is not equal to 0V, the startup time will be always lower.
The startup time is the delay between the negative edge of Enable input (see *SPI Operation Description* on page 3) and the power ON of the output amplifiers.

Note: When the TS4855 is set in full standby mode, Cb is discharged through an internal switch. The time to reach 0 V of Cb voltage with 1µF is about 1ms.

6.6 Pop and Click performance

The TS4855 has internal Pop and Click reduction circuitry. The performance of this circuitry is closely linked with the value of the input capacitor Cin and the bias voltage bypass capacitor Cb.

The value of Cin is due to the lower cut-off frequency value requested. The value of Cb is due to THD+N and PSRR requested always in lower frequency.

The TS4855 is optimized to have a low pop and click in the typical schematic configuration (see *page 2*).

Note: The value of Cs is not an important consideration as regards pop and click.

6.7 Notes on PSRR measurement

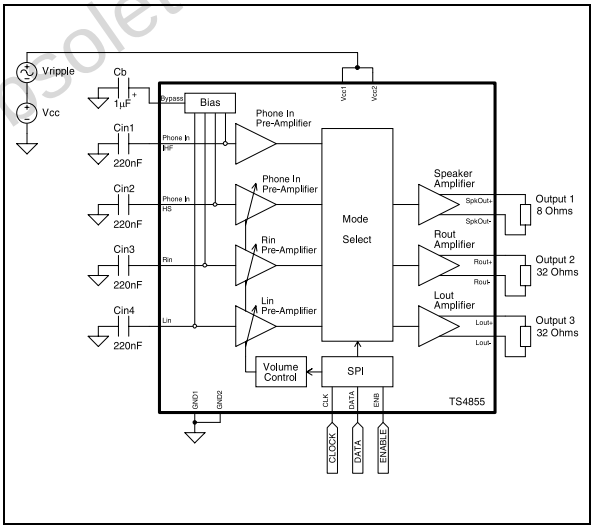
What is the PSRR?

The PSRR is the Power Supply Rejection Ratio. The PSRR of a device, is the ratio between a power supply disturbance and the result on the output. We can say that the PSRR is the ability of a device to minimize the impact of power supply disturbances to the output.

How we measure the PSRR?

The PSSR was measured according to the schematic shown in *Figure 57*.

Figure 57: PSRR measurement schematic



Principles of operation

- The DC voltage supply (Vcc) is fixed.
- The AC sinusoidal ripple voltage (Vripple) is fixed.
- No bypass capacitor Cs is used.

The PSRR value for each frequency is:

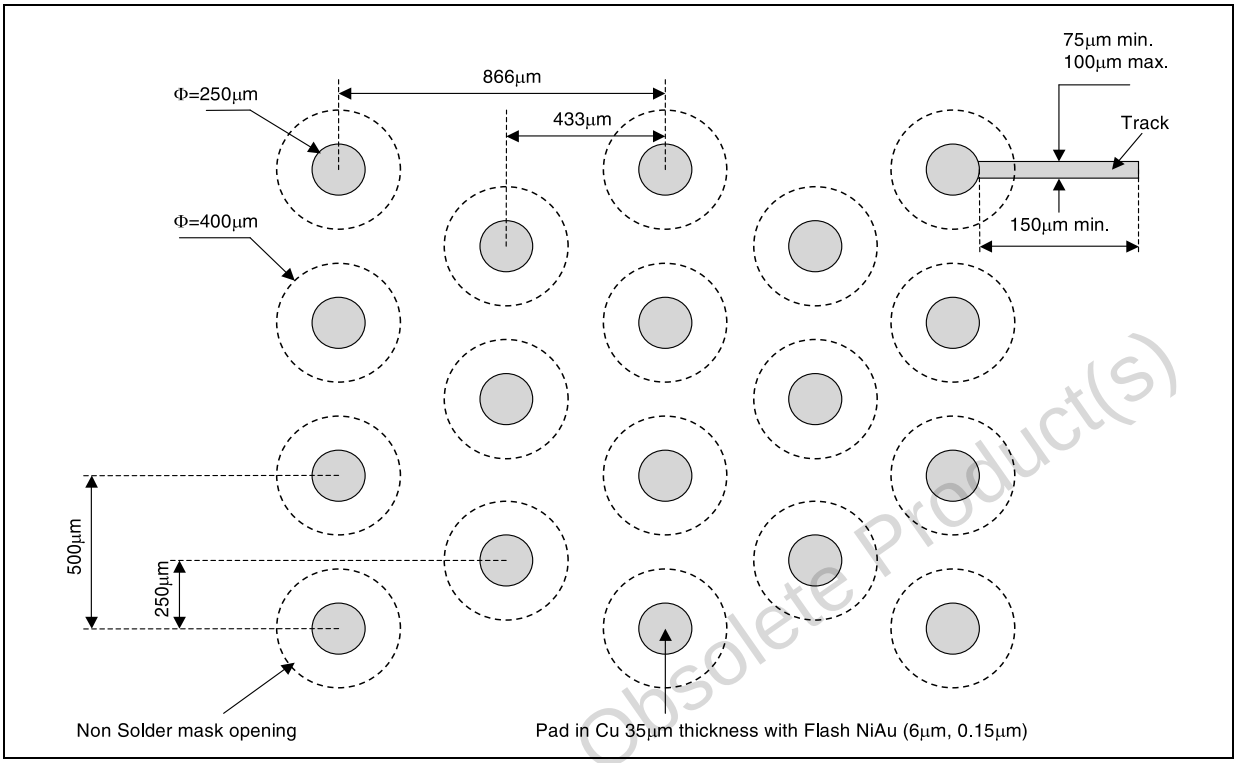
$$PSRR = 20 \times Log\left[\frac{RMS_{(Output)}}{RMS_{(Vripple)}}\right] \quad (dB)$$

Note: The measure of the Rms voltage is a Rms selective measure with a bandpass equal to 1% of the measured frequency .

6.8 Power-On Reset

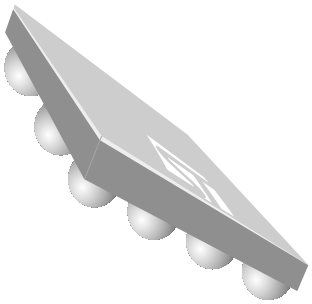
When Power is applied to Vdd, an internal Power On Reset holds the TS4855 in a reset state until the Supply Voltage reached its nominal value.
The Power On reset has a typical threshold at 1.8V.

Figure 58: TS4855 Footprint Recommendation



7 PACKAGE INFORMATION

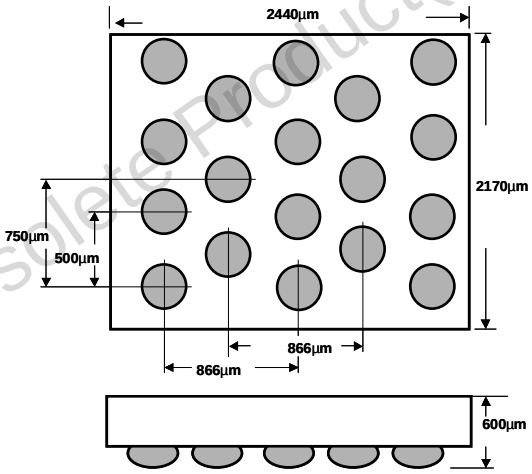
Flip-chip package—18 bumps: TS4855IJT



Marking (on top view)

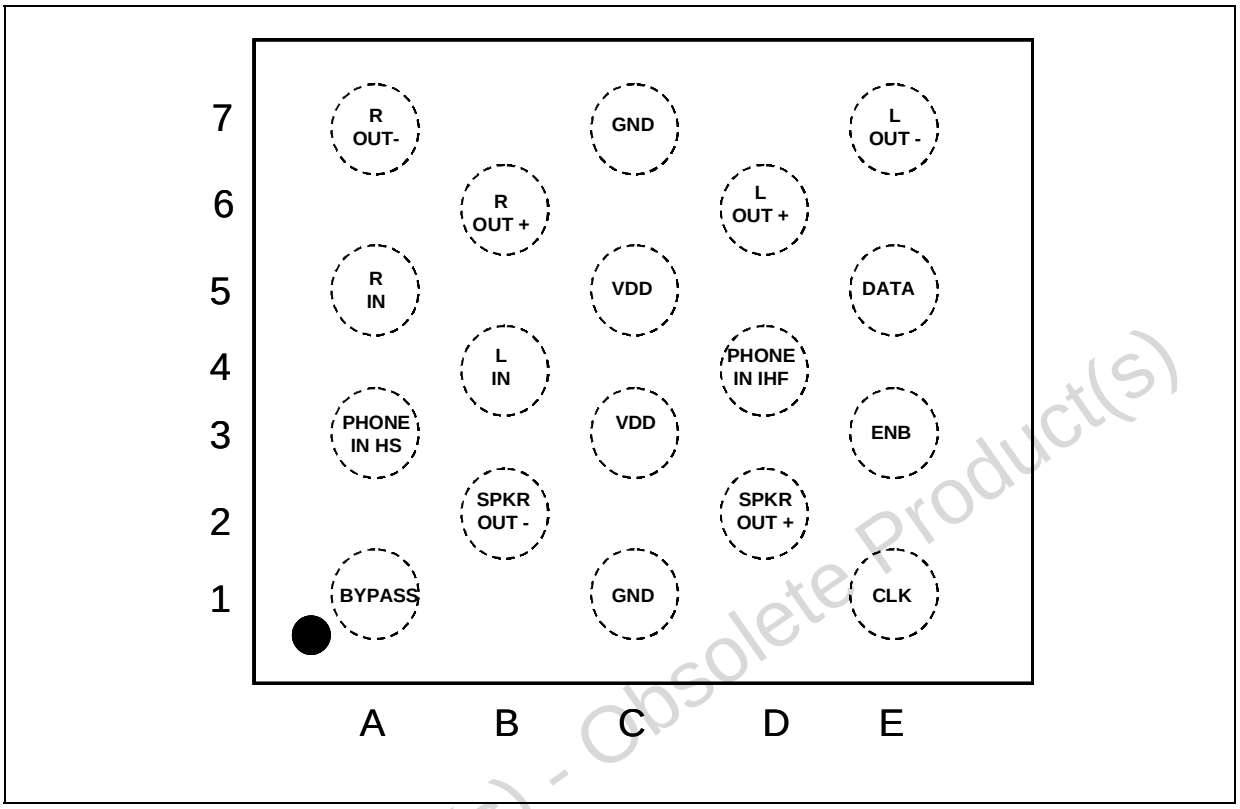
- ST LOGO
- Part number: B55
- Three digit Datecode: YWW
- The dot is for marking the bump1A

Package mechanical data



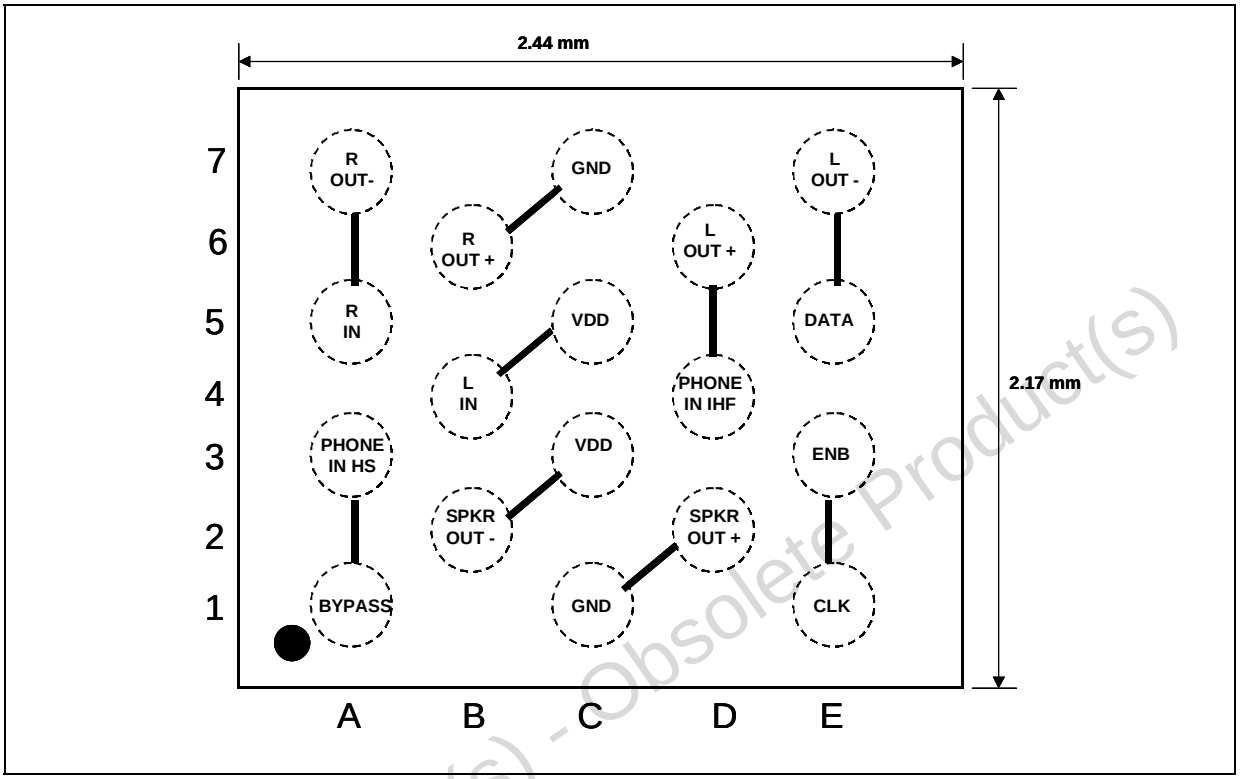
- Die size: **2440µm x 2170µm ±30µm**
- Die height (including bumps): **600µm**
- Nominal Bumps diameter: 315µm ±10µm
- Nominal Bumps height: **250µm** ±10µm
- Pitch: **500µm** ±10µm
- Die Height : **350µm** ±20µm

Pin out (top view)



Daisy chain mechanical data

All drawings dimensions are in millimeters



Remarks

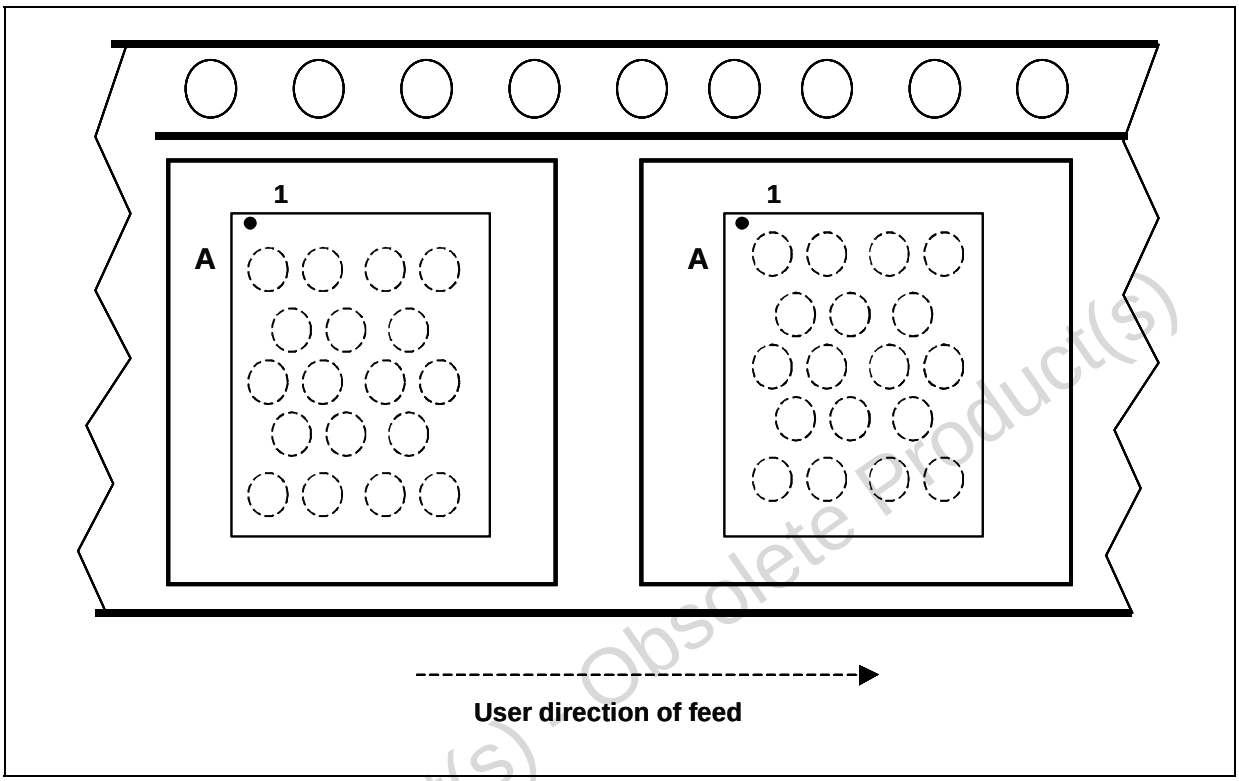
Daisy chain sample is featuring pin connection two by two. The schematic above is illustrating the way connecting pins each others. This sample is used for testing continuity on board. PCB needs to be designed on the opposite way, where pin connections are not done on daisy chain samples. By that way, just connecting a Ohmmeter between pin 1A and pin 5A, the soldering process continuity can be tested.

Order code

Part Number	Temperature Range	Package	Marking
		J	
TSDC02IJT	-40, +85°C	•	DC2

8 TAPE & REEL SPECIFICATION

Figure 59: Top view of tape & reel



Device orientation

The devices are oriented in the carrier pocket with bump number A1 adjacent to the sprocket holes.